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FROM: MARK JOY
REGISTRATION NO. 35,562

DIRECT LINE: 312 616 5673

TO: EXAMINER LAZARO
GROUP 2155
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C.

TELEPHONE NUMBER: NOT AVAILABLE
FACSIMILE NUMBER: 703 872 9306

APPEAL BRIEF AND TRANSMITTAL

IN RE APPLN. OF:	PHILLIPS ET AL.
APPLICATION NO.	09/638,774
FILED:	AUGUST 15, 2000
FOR:	NETWORK SERVER CARD AND METHOD FOR HANDLING REQUESTS...
GROUP ART UNIT:	2155
EXAMINER:	LAZARO

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PATENT
Attorney Docket No. 205225

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Robert C. Phillips, et al.

Application No. 09/638,774

Filed: August 15, 2000

For: A Network Server Card and Method for Handling Requests Received Via A Network Interface

Art Unit: 2155

Examiner: Lazaro, David R.

TRANSMITTAL OF
APPELLANTS' APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with 37 CFR 41.37, appellants hereby submit Appellants' Brief on Appeal.

The items checked below are appropriate:

1. **Status of Appellants**

This application is on behalf of ☐ other than a small entity or ☒ a small entity.

2. **Fee for Filing Brief on Appeal**

Pursuant to 37 CFR 41.20(2), the fee for filing the Brief on Appeal is for: ☐ other than a small entity or ☒ a small entity.

Brief Fee Due $250.00

3. **Oral Hearing**

☐ Appellants request an oral hearing in accordance with 37 CFR 41.47.

A separate paper requesting oral hearing is attached.

4. **Extension of Time**

☒ Appellants petition for a three-month extension of time under 37 CFR 1.136, the fee for which is $510.00.

☒ Appellants believe that no extension of time is required. However, this conditional petition is being made to provide for the possibility that appellants have inadvertently overlooked the need for a petition and fee for extension of time.

Extension fee due with this request: $510.00

In re Appln. of Robert C. Phillips, et al.
Application No. 09/638,774

5. Total Fee Due

The total fee due is:

Brief on Appeal Fee	$250.00
Request for Oral Hearing	$ 0.00
Extension Fee (if any)	$510.00

Total Fee Due: $760.00

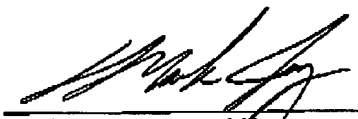
6. Fee Payment

☐ Attached is a check in the sum of $
☒ Charge Account No. 12-1216 the sum of $760.00. A duplicate of this transmittal is attached.

7. Fee Deficiency

☒ If any additional fee is required in connection with this communication, charge Account No. 12-1216. A duplicate copy of this transmittal is attached.

Respectfully submitted,



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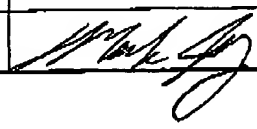
Date: April 22, 2005

CERTIFICATE OF MAILING OR TRANSMISSION UNDER 37 CFR 1.8			
I hereby certify that this APPEAL BRIEF TRANSMITTAL AND APPEAL BRIEF (along with any documents referred to as attached or enclosed) are, on the date indicated below, ☐ being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop , Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or ☒ being facsimile transmitted to the U.S. Patent and Trademark Office, Attention: Examiner Lazaro, Art Unit 2155, Facsimile Number 703 872-9306.			
Name (Print/Type)	Mark Joy		
Signature		*Date*	April 22, 2005

COPY

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Attorney Docket No. 205225

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Art Unit: 2155

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In re Appln. of Robert C. Phillips, et al.
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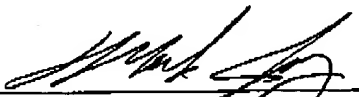

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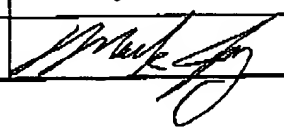
Name (Print/Type)	Mark Joy		
Signature		*Date*	April 22, 2005

PATENT
Attorney Docket No. 205225

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Robert C. Phillips, et al.

Art Unit: 2155

Application No. 09/638,774

Examiner: Lazaro, David R.

Filed: August 15, 2000

For: A Network Server Card and Method for Handling Requests Received Via A Network Interface

APPELLANTS' APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In support of the appeal from the final rejection dated June 22, 2004, Appellants now submit their Brief.

Real Party In Interest

The patent application that is the subject of this appeal was originally assigned to Ikadega, Inc. and is presently believed to be the owner of this application.

Related Appeals and Interferences

There are no appeals or interferences that are related to this appeal.

Status of Claims

Currently pending claims 1-24 presently stand rejected. All the currently pending claims are being appealed.

In re Appln. of Robert C. Phillips, et al.
Application No. 09/638,774

Status of Amendments

There have been no amendments filed subsequent to the final rejection.

Summary of Claimed Subject Matter

The claimed invention set forth in **independent claim 1** is directed to a distributed multiprocessor server system (see, FIG. 1) that facilitates delegating processing of at least portions of requests embedded within request messages received via a network interface (network interface 12; p. 12, ll. 3-15). An intelligent switch (packet classifier and switch 24; p. 14, ll. 5-16), coupled to the network interface, comprises logic components for identifying a new request that has been received via the network interface.

Claim 1 further recites a default handler processor (default network processor 16, p. 13, l. 18 to p. 14, l. 2, and p. 14, l. 17 to p. 15, l. 4). The default handler processor associates a request type with at least a portion of the new request, identifies a handler processor from a set of specialized handler processors (specialized handler processors 26, p. 14, ll. 18-21 and p. 17, lines 12-22) based upon the request type, and issues a message reassigning the new request to the identified handler processor (p. 31, ll. 12-23). A bus structure links the set of specialized handler processors (26) to the intelligent switch (24). Request reassignment tracking logic within the switch (p. 30, ll. 8-14) enables the intelligent switch to route messages associated with the reassigned request between the identified handler processor (of the specialized handler processors 26) and the network interface (12). The recited functional components facilitate completing the new request through communications between the identified handler of specialized handler processors (26) and the network interface (12) via the intelligent switch (24) without intervention by the default handler processor (16).

Regarding **independent claim 13**, a method (summarized in FIG. 4) is recited for receiving requests in a multiprocessor network server (see, FIG. 1) including a network interface (12), an intelligent switch (24), a default handler processor (16), and a set of specialized handler processors (26). The method comprises receiving, by the network interface, a message packet including a request and passing the request to the intelligent switch (step 100, p. 30 ll. 5-8).

The intelligent switch determines the request is a new request (step 102, p. 30, ll. 8-10), and in response performs a set of additional steps. The default handler processor (16) identifies, based upon a request type of the new request, a handler processor from the set of specialized handler processors that is capable of executing at least a portion of the new request (step 116, p. 31, ll. 13-23). The new request is reassigned to the identified handler processor to perform the new request (step 116, p. 31, ll. 13-15). The intelligent switch creates a request table entry identifying the request and the identified handler processor to which the new request is reassigned (step 116, p. 31, ll. 17-20).

Thereafter, the identified handler processor executes at least the portion of the new request. During the executing step the identified handler processor communicates with the network interface via the intelligent switch, thereby bypassing the default handler processor while executing at least the portion of the new request (step 118, p. 31, l. 23 to p. 32, l. 3).

Grounds of Rejection to be reviewed on Appeal

Appellants appeal the rejection of claims 1, 2, 7, 9, 11, 12, 13, 14, 19, 21, 23 and 24 as anticipated, under 35 U.S.C. Section 102(a), by Rierden et al. U.S. Patent 5,978,577.

Appellants appeal the rejection of claims 3 and 15 as obvious, under 35 U.S.C. Section 103(a), over Rierden in view of Basham et al. U.S. Patent 6,425,059.

Appellants appeal the rejection of claims 4 and 16 as obvious, under 35 U.S.C. Section 103(a), over Rierden in view of Basham and Jacobson et al. U.S. Patent 5,546,558.

Appellants appeal the rejection of claims 5 and 17 as obvious, under 35 U.S.C. Section 103(a), over Rierden in view of Rungta U.S. Patent 6,484,186.

Appellants appeal the rejection of claims 6, 8, 10, 18, 20, and 22 as obvious, under 35 U.S.C. Section 103(a), over Rierden in view of Lim U.S. Patent 6,374,296.

In re Appln. of Robert C. Phillips, et al.
Application No. 09/638,774

Argument

I. The rejection of claims 1, 2, 7, 9, 11, 12, 13, 14, 19, 21, 23 and 24 as anticipated, under 35 U.S.C. Section 102(a), by Rierden et al. U.S. Patent 5,978,577.

Appellants appeal the rejection, of Claims 1, 2, 7, 9, 11, 12, 13, 14, 19, 21, 23, and 24 under Section 102(a) as being anticipated by Rierden because one or more of the recited elements of independent claims 1 and 13 are not present in the Rierden patent.

A. CLAIM 1

The invention recited in claim 1 is directed to a distributed multiprocessor architecture including:

- an intelligent switch that receives/recognizes all incoming new requests from a WAN bus interface;
- a default network processor that receives all initial requests (intelligently directed by the intelligent switch), determines the type of request (e.g., file transfers of particular types – as specified, by way of example on page 17 of the application), and delegates the request to one of a set of specialized request handlers; and
- bus structure and request reassignment tracking logic that support *completing at least the portion of the new request through communications between the identified handler of specialized handler processors and the network interface via the intelligent switch without intervention by the default handler processor.*

Appellants submit that the italicized text, recited from the last clause of claim 1, in combination with the other recited elements of claim 1, defines a structural relationship and functional capability that define the capability of the claimed invention to by-pass the default handler processor, which initially set up a connection to a specialized handler processor in response to a new request, during a completion phase of servicing the received request.

Addressing the Final Office action's comments at the top of page 14, Appellants submit that "without intervention by the default handler processor" does not entail the "pass through" mode described in Rierden since the act of passing the results through the DDS consumes processor assets (bus cycles, memory, etc.). Appellants note that the first definition of "intervene", "to come, be, or lie between" in Webster's New World Dictionary (Second College Edition) is clearly the appropriate definition in view of the disclosure of the present application.

Thus, as recited in claim 1, requests are completed without the default handler processor coming between communications between the identified handler processor and the network interface. In contrast to the recited invention, the distributed multiprocessor architecture in Rierden comprises one or more data directory servers (DDSs) that are interposed between a set of servers that actually carry out a request and a network interface through which clients submit the requests.

Appellants submit that the Final Office Action's reliance, at the bottom half of page 13, upon a "logical" separation of the RPC handler function from the DDS ignores structural elements described in the specification and recited in claim 1 – in particular, physically separating the intelligent switch (for routing communications between the processors and the network interface) from the default handler processor. Appellants' entire architecture is premised upon eliminating a physical bottleneck potentially presented by the default handler processor during the completion of requests. This aim cannot be achieved by mere "logical" separation of these two specifically recited structural elements of the claimed invention. Therefore, Appellants specifically object to this explanation/basis for the Final Office Action's rejection of claim 1.

In summary, Rierden's disclosed system Rierden does not disclose that the recited "bus structure" and "request reassignment tracking logic" enable completing subsequent communications between the handler processors (data servers 160) and the network interface (105) *"without intervention by the default handler processor"* (DDS 150). Instead, the system disclosed in Rierden appears to require all communications to *pass through* the DDS 150 (see, col. 17, lines 16-18). For at least this reason, claim 1 is not anticipated by Rierden.

B. CLAIM 13

Appellants object to the Final Office Action's rejection of independent method claim 13 for at least the reasons set forth above with regard to claim 1 inasmuch as the communications between an identified handler processor and a network interface do not bypass the default handler processor as called for in claim 13. Rierden does not disclose an intelligent switch, bus, and multiprocessor arrangement that would support the recited steps including "executing, by the identified handler processor, at least the portion of the new request, wherein during the executing step the identified handler processor communication with the network interface via the intelligent switch; thereby bypassing the default handler processor while executing at least a portion of the new request" – as recited in claim 13. The Final Office Action, at pages 14-15

does not acknowledge that claim 13 calls for communications between the identified handler and the network interface while executing *a portion of the new request* and bypassing the default handler processor while executing *the portion of the new request.*

Appellants traverse the rejection of dependent claims 2, 7, 9, and 12 and 14, 19, 21 and 24 for at least the reason that Rierden does not disclose a non-blocking switch interposed between a DDS 150 and the Data server(s) 160. Appellants specifically object to the Final Office Action's unduly broad interpretation of "non-blocking" when non-blocking should be given its ordinary, clear meaning. The Final Office Action identifies portions of Rierden that indicate a high bandwidth, but do not disclose or suggest the recited "non-blocking" element.

C. CLAIMS 11 and 23

Furthermore, Appellants object to the continued rejection of claims 11 and 23. Appellants previously requested identification of claim 11 and claim 23 recited structure specifically within Rierden. The Appellants specifically object to the Final Office Action's assertion that such structure is *typically/inherently* present in the Rierden system. However, there is not basis in the cited references for proposing such conclusions. It is just as (if not more) likely that no buffer is present. In such case, the recited structure is not inherent.

II. The rejection of claims 3 and 15 as obvious, under 35 U.S.C. Section 103(a), over Rierden in view of Basham et al. U.S. Patent 6,425,059.

Appellants traverse the rejection of Claims 3 and 15 under Section 103(a) as being unpatentable over Rierden in view of Basham. While not contending that version controlled partitions are new, Appellants respectfully submit that using the recited multiprocessor architecture to provide access to such a data storage facility type is neither disclosed nor suggested in the prior art. Appellants respectfully submit that their previous grounds for traversing the rejection acknowledged their inability to discern any suggestion to incorporate the secondary reference's teachings into the system disclosed in Rierden. Where is the teaching to modify Rierden to incorporate the combination of elements recited in claims 3 and 15?

III. The rejection of claims 4 and 16 as obvious, under 35 U.S.C. Section 103(a), over Rierden in view of Basham and Jacobson et al. U.S. Patent 5,546,558.

Appellants traverse the rejection of Claims 4 and 16 under Section 103(a) as being unpatentable over Rierden in view of Basham and Jacobson. In particular, Appellants respectfully submit that the prior art does not disclose using the recited multiprocessor architecture to provide access to a data storage facility that supports incorporating a straddle into storage partitions to facilitate copying stored data assets while maintaining the availability of the stored asset while the data is being copied to a new location. Where is the teaching to modify Rierden to incorporate the combination of elements recited in claims 4 and 16?

IV. The rejection of claims 5 and 17 as obvious, under 35 U.S.C. Section 103(a), over Rierden in view of Rungta U.S. Patent 6,484,186.

Appellants traverse the rejection of Claims 5 and 17 under Section 103(a) as being unpatentable over Rierden in view of Rungta. Appellants respectfully submit that the prior art does not disclose using the recited bit-map entries to represent the current state of files within the data storage facility that is accessed via the multiprocessor architecture recited in claimed combinations. Where is the teaching to modify Rierden to incorporate the combination of elements recited in claims 5 and 17?

V. The rejection of claims 6, 8, 10, 18, 20, and 22 as obvious, under 35 U.S.C. Section 103(a), over Rierden in view of Lim U.S. Patent 6,374,296.

Appellants traverse the rejection of Claims 6, 8, 10, 18, 20 and 22 under Section 103(a) as being unpatentable over Rierden in view of Lim. Appellants respectfully submit that while each of the elements, by themselves, may be known, the prior art does not disclose or suggest incorporating the recited elements into a system including the multiprocessor architecture recited within each of these claims. Again, the Final Office Action does not identify the teachings in the cited references that suggest their combination to render the claimed invention. The mere existence of an element in an identified reference alone does not support a conclusion of obviousness. If that was the case, every combination of known elements, regardless of how they are combined, would be obvious.

In re Appln. of Robert C. Phillips, et al.
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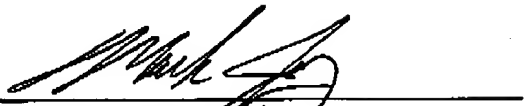
Respectfully submitted,



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Date: April 22, 2005

205225 Appeal Brief

Claims Appendix

1. A distributed multiprocessor server system for facilitating delegated processing of at least portions of requests associated with request messages received via a communicatively coupled network link, the system comprising:

a network interface;

an intelligent switch coupled to the network interface, the switch comprising logic components for identifying a new request, corresponding to a message packet received by the network interface, passed from the network interface to the intelligent switch;

a default handler processor coupled to the intelligent switch and configured to receive the new request from the intelligent switch, the default handler processor comprising delegation logic facilitating: associating a request type with at least a portion of the new request, identifying a handler processor from a set of specialized handler processors for executing at least the portion of the new request based upon the request type, and issuing a message reassigning at least the portion of the new request to the identified handler processor; and

at least one bus structure communicatively linking the set of specialized handler processors to the intelligent switch and request reassignment tracking logic enabling the intelligent switch to route messages associated with at least the portion of the reassigned request between the identified handler processor and the network interface, thereby facilitating completing at least the portion of the new request through communications between the identified handler of specialized handler processors and the network interface via the intelligent switch without intervention by the default handler processor.

2. The distributed multiprocessor server system of claim 1 further comprising a storage server system linked to the intelligent switch via a non-blocking switch.

3. The distributed multiprocessor server system of claim 2 wherein the storage server system comprises memory arranged as a set of version controlled partitions.

4. The distributed multiprocessor server system of claim 3 wherein a straddle is incorporated into a partition, thereby facilitating continuous availability of all stored data while a particular partition is relocated within the storage server system.

5. The distributed multiprocessor server system of claim 2 wherein a state of a file maintained by the storage server system is represented in the form of a bitmap entry; and wherein a first bit is associated with a creator of new data in the file and a second bit is associated with a deleter of data stored in the file.

6. The distributed multiprocessor server system of claim 2 wherein the intelligent switch receives messages from the non-blocking switch in the form of ATM cells.

7. The distributed multiprocessor server system of claim 2 wherein the set of specialized handler processors includes a processor facilitating transfer of a file stored on the storage server system.

8. The distributed multiprocessor server system of claim 7 wherein the file transfer is performed in accordance with a TCP named file transfer protocol over an identified connection.

9. The distributed multiprocessor server system of claim 2 wherein the set of specialized handler processors includes a processor including functionality facilitating transforming the data within a file prior to transfer.

10. The distributed multiprocessor server system of claim 1 wherein the set of specialized handler processors includes a processor including computer gateway interface (CGI) functionality.

11. The distributed multiprocessor server system of claim 1 further comprising a data retrieval buffer interposed between a data storage facility and the set of specialized handler processors, the data retrieval buffer being independently accessible with respect to a primary RAM utilized by the default handler processor.

12. The distributed multiprocessor server system of claim 1 further comprising new/old request differentiation logic enabling the server system to identify and respond to new connection requests at a different level of priority than a priority assigned to requests associated with existing connections.

13. A method for allocating received requests in a multiprocessor network server including a network interface, an intelligent switch, a default handler processor, and a set of specialized handler processors, the method comprising the steps of:

receiving, by the network interface, a message packet including a request;

passing at least the request to the intelligent switch;

determining the request is a new request, and in response performing the further steps of:

identifying by the default handler processor, based upon a request type of the new request, a handler processor from the set of specialized handler processors that is capable of executing at least a portion of the new request, and

reassigning by the default handler processor, the new request to the identified handler processor to perform at least a portion of the new request, wherein the intelligent switch creates a request table entry identifying the request and the identified handler processor to which at least a portion of the new request is reassigned; and

executing, by the identified handler processor, at least the portion of the new request, wherein during the executing step the identified handler processor communicates with the network interface via the intelligent switch; thereby bypassing the default handler processor while executing at least the portion of the new request.

14. The method of claim 13 wherein a storage server system is linked to the intelligent switch via a non-blocking switch, and the executing step comprises transferring data from the storage server to the network interface.

15. The method of claim 14 further comprising arranging stored content within the storage server system as a set of version controlled partitions.

16. The method of claim 15 further comprising incorporating a straddle into a partition, thereby facilitating continuous availability of all stored data while a particular partition is relocated within the storage server system.

17. The method of claim 14 further comprising maintaining, by the storage server system, a state of a file in the form of a bitmap entry; and wherein a first bit is associated with a creator of new data in the file and a second bit is associated with a deleter of data stored in the file.

18. The method of claim 14 further comprising receiving, by the intelligent switch, a message from the non-blocking switch in the form of ATM cells.

19. The method of claim 14 further comprising providing, within the set of specialized handler processors, a processor facilitating transfer of a file stored on the storage server system.

20. The method of claim 19 wherein the processor facilitating transfer of a file operates in accordance with a TCP named file transfer protocol over an identified connection.

21. The method of claim 14 further comprising providing, within the set of specialized handler processors, a processor including functionality facilitating transforming the data within a file prior to transfer.

22. The method of claim 13 further comprising providing, within the set of specialized handler processors, a processor including computer gateway interface (CGI) functionality.

23. The method of claim 13 further comprising storing data retrieved from a data storage facility in a data retrieval buffer interposed between a data storage facility and the set of specialized handler processors, the data retrieval buffer being independently accessible with respect to a primary RAM utilized by the default handler processor.

24. The method of claim 13 further comprising differentiating a new connection request from a request associated with an existing connection, thereby facilitating assigning a first priority to the request associated with the existing connection and a second priority to the new connection request.